Analog circuit design

Amplifier is a key module in the design of analog integrated circuit, which has a wide range of applications. A differential input single output CMOS amplifier with voltage gain no less than 30dB is designed in standard CMOS process. Based on the selected process, the higher the gain bandwidth product is, the better the power consumption is under the premise of ensuring sufficient phase margin.

(1) Based on cadence or other EDA software, the graphic input editing and pre simulation verification of the circuit are completed.

(2) Based on cadence or other EDA software, the layout design, physical verification, parameter extraction and post simulation are completed on the basis of (1).

Main design specifications: a differential input single output CMOS amplifier with voltage gain no less than 30dB is designed in standard CMOS process. Based on the selected process, the higher the gain bandwidth product is, the better the power consumption is under the premise of ensuring sufficient phase margin.

**Main steps and results**

(1) Circuit structure

CMOS single ended output differential amplifier with a mirror current source. As shown in Figure 1:

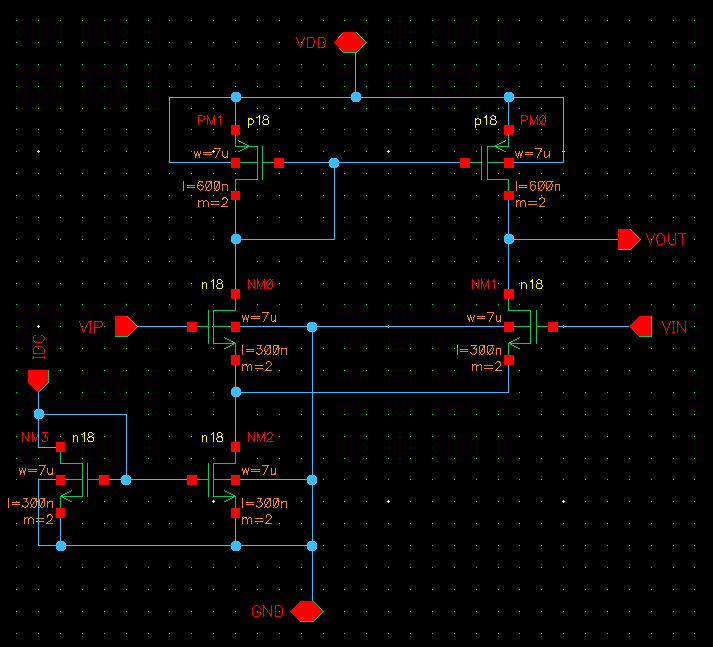
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Figure 1. Circuit structure

(2) Circuit parameters

According to the analog circuit theory, based on the circuit performance index, the device parameters are set as follows: NMOS transistors are designed with gate length of 0.3 um and gate width of 7 um with multiplier of 2; PMOS transistors are designed with gate length of 0.6 um and gate width of 7 um and multiplier of 2.

(3) Pre circuit simulation process

In analog integrated circuit, pre simulation is a very important part. Pre simulation simulates the function of the circuit, forms feedback according to the simulation results, and then optimizes the design parameters of the circuit, and finally makes the performance parameters of the circuit reach the optimal.

Before the layout design is completed, the simulation of the circuit is ideal, which does not contain any physical information such as parasitic effect and interconnect delay, which is called "pre simulation".

Before the simulation, we must first establish a symbol, define pins and input and output signals, define Vdd and GND, VIN and Vout, and draw the circuit symbols of the circuit schematic diagram shown in Figure 1, as shown in Figure 2

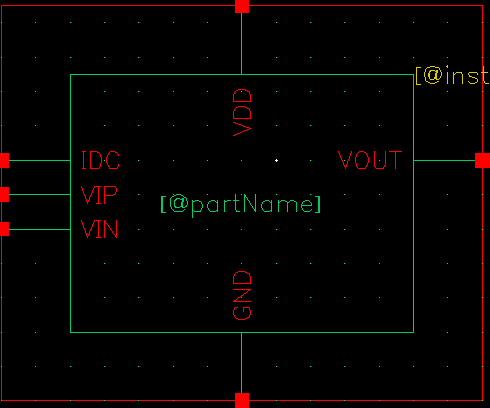


Figure 2. Symbol of circuit diagram

After the excitation signal is added outside the symbol, the pre simulation can be started. The circuit used in the pre simulation is shown in Fig. 3

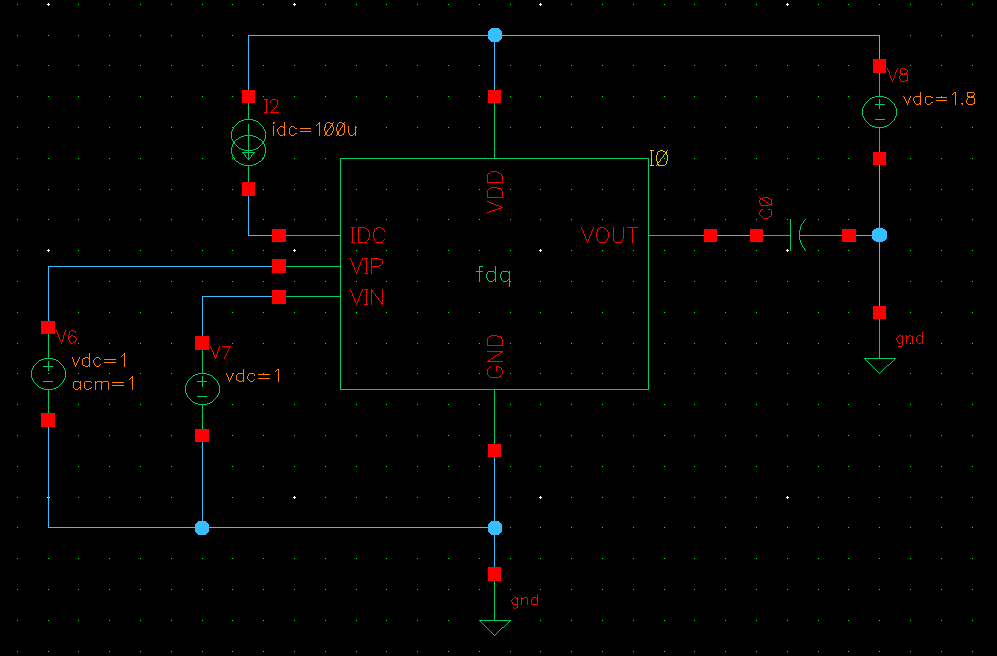


Figure 3. Pre simulation test circuit

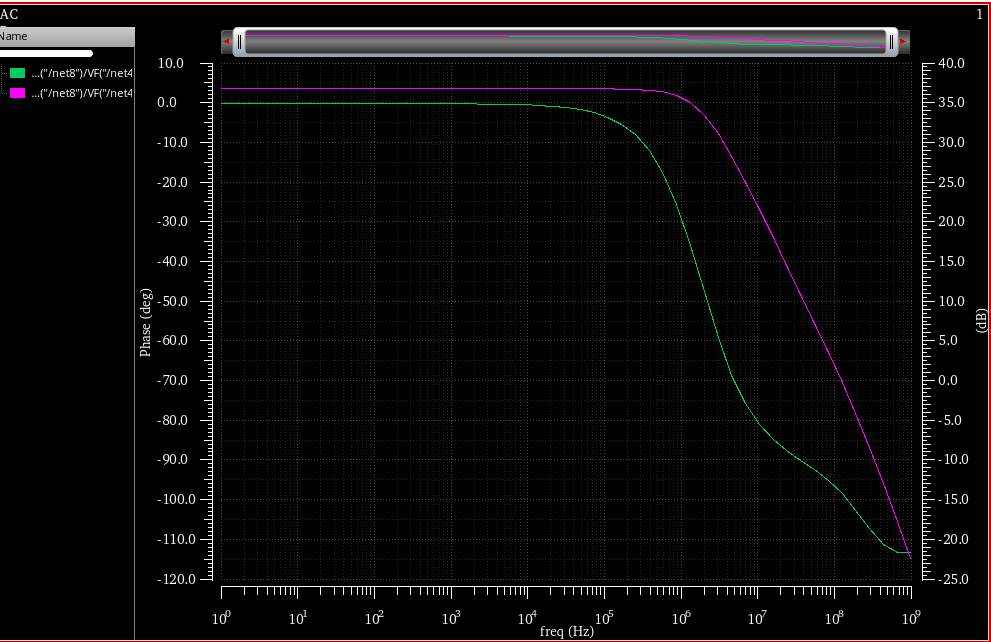
The power supply voltage is defined as 1.8V and the current source IDC is 0.1mA

Figure 4. Pre simulation results

Among them, the power supply voltage is set to 1.8V, the current source IDC is 0.1mA, Vin is connected to DC voltage of 0.9V, VIP is connected to 0.9V, and AC magnet is 1V.

According to the simulation results, a series of performance parameters are extracted: the low-frequency amplification factor is 37.9dB, the gain broadband product is 123MHz, and the phase margin is 84 °.

Next, transient simulation is carried out. Transient simulation can obtain the characteristics of signal changing with time. The circuit diagram used for transient simulation of the circuit is shown in Figure 5

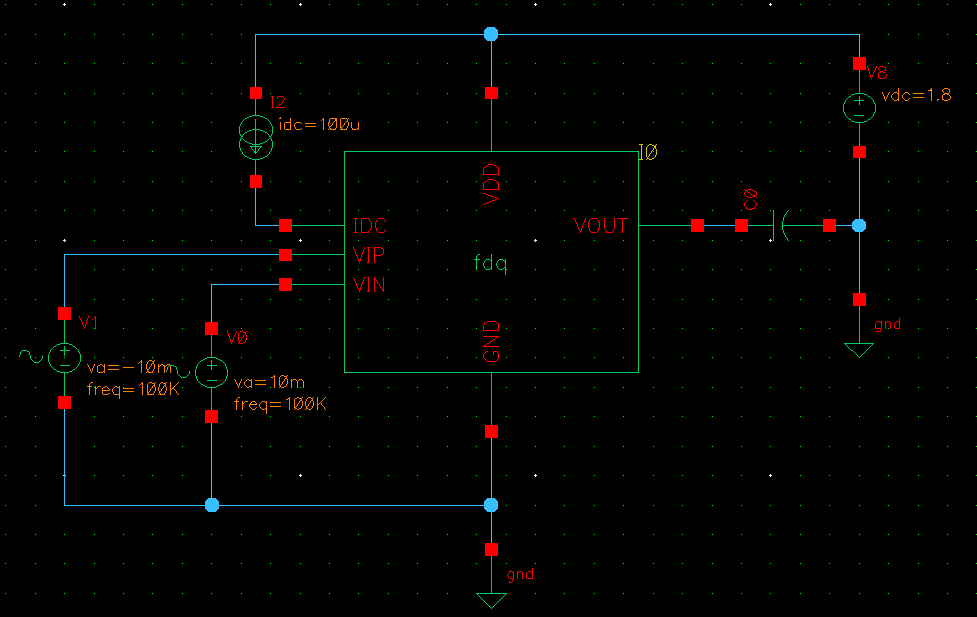
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Figure 5. Transient simulation circuit diagram

The output load capacitor C0 is 1pf, IDC is 0.1mA, VIP and VIN are a pair of differential mode sinusoidal signals, the frequency is 100KHz, and the DC offset is 0.9V

The transient simulation results are shown in Figure 6

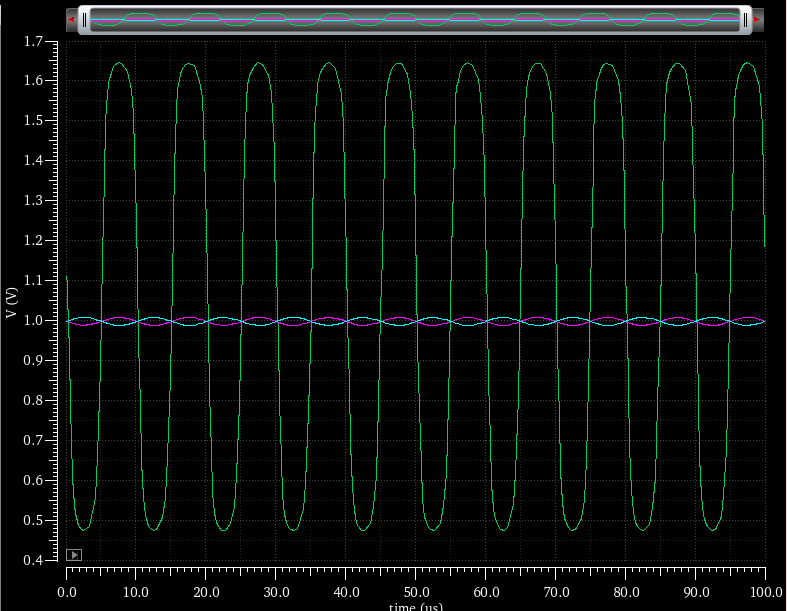
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Figure 6. Transient simulation results

(4) Circuit layout design

In circuit design, schematic design and function simulation are not enough. If we want to turn the theoretical circuit into practical circuit, we must convert the circuit schematic into layout. The layout design is related to the final realization of the circuit, and has a great impact on the circuit performance, cost and other parameters, and even affects the actual circuit function. In the layout design, the first thing to consider is to make a trade-off between the layout area and circuit performance under the condition of ensuring that the circuit function is not affected. The optimization of layout, wiring and other factors is mainly considered The matching of resistance and capacitance, parasitic effect and other issues need to be considered comprehensively. According to different process requirements, the drawing method of layout is also different. The 0.18um standard CMOS process library provided by SMIC is used to design the layout.

According to the process requirements, the minimum spacing and width of the first metal layer is 0.23um, the minimum area is 0.2um, the minimum spacing and width of the second metal layer is 0.28um, and the minimum spacing between through holes is 0.25um.

The layout of the circuit is shown in Figure 7：

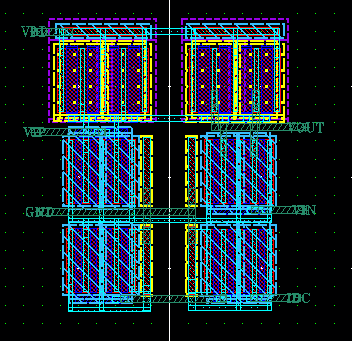


Figure 7. Layout design

In the layout design of differential circuit, the most important thing is to ensure the MOS matching with the transistor. If the MOSFET does not match, the common mode signal will be amplified, which is a very bad situation. Among them, the wiring should be as straight and symmetrical as possible, the internal signal should be metal 1, and the signal line connected with the outside should be metal 2. Because the current in the metal wire will produce electric field, which will affect the work of MOS transistor, the metal wiring should avoid passing through the active area and gate of MOS transistor. Finally, define the input and output, power supply, ground port and so on.

(5) DRC, LVS validation

DRC verification: DRC (design rules check) is a kind of checking work completed by computer, which usually appears in EDA (Electronic Design Automation) software.

DRC verification of the above layout design is shown in Figure 8:

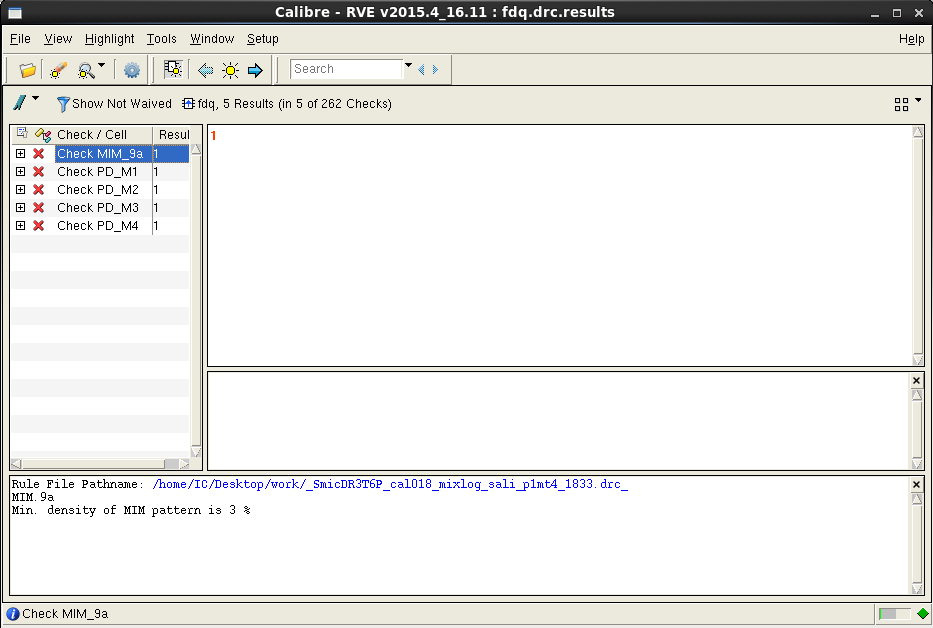


Figure 8. DRC verification results

From the DRC verification results, there are five errors, but we can see that they are all metal density errors, which are related to the actual process production and can be ignored in the simulation. In addition, no other errors were found, which means DRC validation passed.

LVS verification: LVS, full name of layout versus schemes, is the verification tool of Dracula, which is used to verify whether the layout and logic diagram match. LVS compares layout and logic connectivity at the transistor level and outputs all inconsistencies.

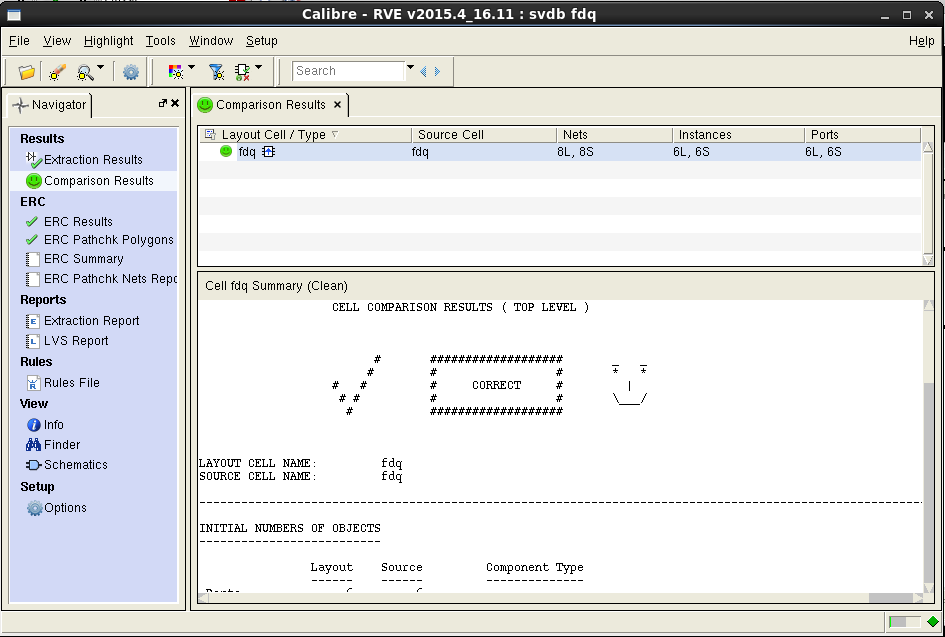
DRC verification aims at whether the layout design matches with the actual process, while LVS verification aims at verifying whether the layout is consistent with the schematic. Cadence compares the web labels extracted from the layout with those extracted from the schematic. If they are consistent, LVS verification is passed. The results of LVS verification are shown in Figure 9****

Figure 9. LVS verification results

A smiling face appears in the verification result, indicating that LVS verification is passed.

(6) Post simulation

After the layout design is completed, the MOS integrated circuit in the form of layout is obtained. It is a complex system composed of diffusion layer, dielectric layer, polysilicon layer and metal layer.

With the continuous progress of technology, parasitic effects such as parasitic resistance, parasitic capacitance and interconnect delay can not be ignored, especially for deep submicron IC design.

"Post simulation" refers to that after the layout design is completed, the parasitic parameters and interconnection delay are inversely labeled into the extracted circuit network table for simulation, and the circuit is analyzed to ensure that the circuit meets the design requirements. The method used in the post simulation is not different from that in the former simulation, only parasitic parameters and interconnection delay are added. If the post simulation can get the correct results, we can safely deliver the layout data to foundry.

The parasitic parameters extracted by the circuit are shown in figures 10 and 11:

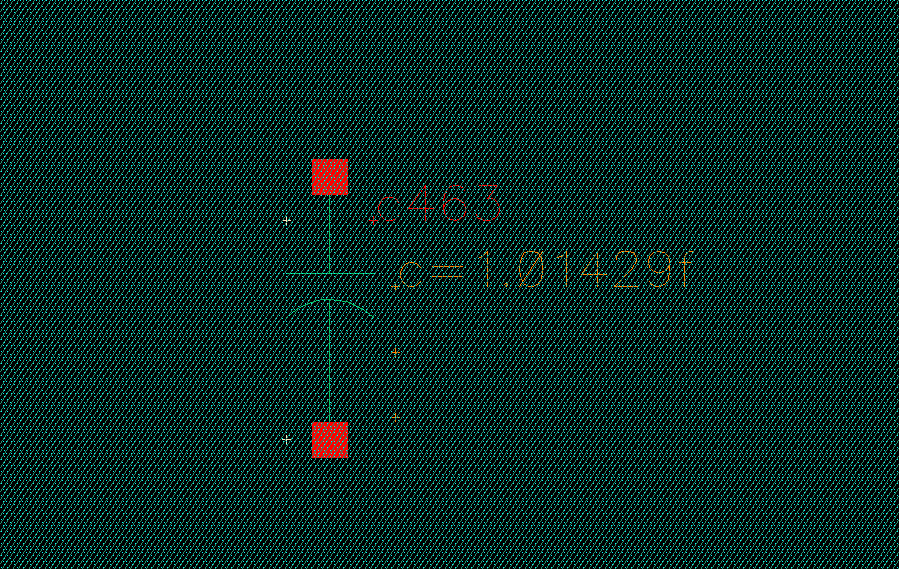


Figure 10. Extraction of parasitic capacitance parameters

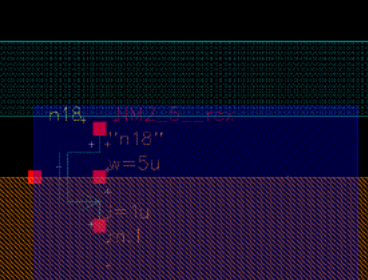
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Figure 11. Extraction of parasitic parameters of MOS transistor

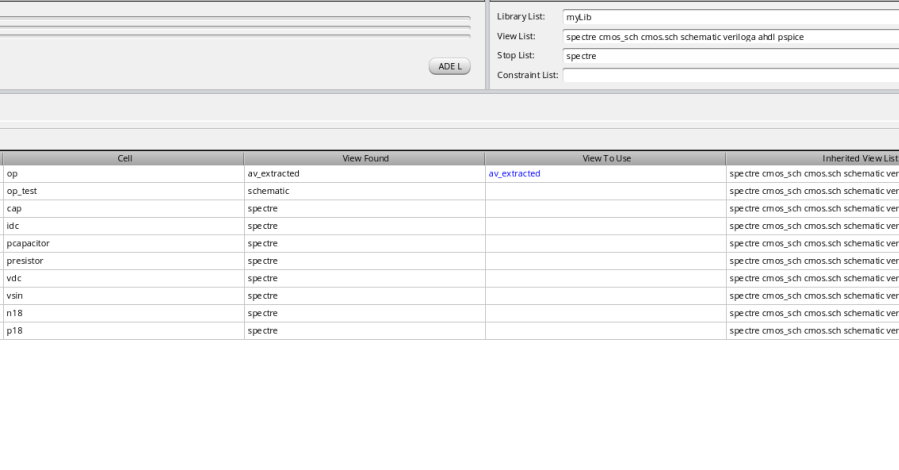
After extracting the parasitic parameters, the simulation results are shown in FIG. 12 and FIG. 13 ****

Figure 12. Post simulation results 1

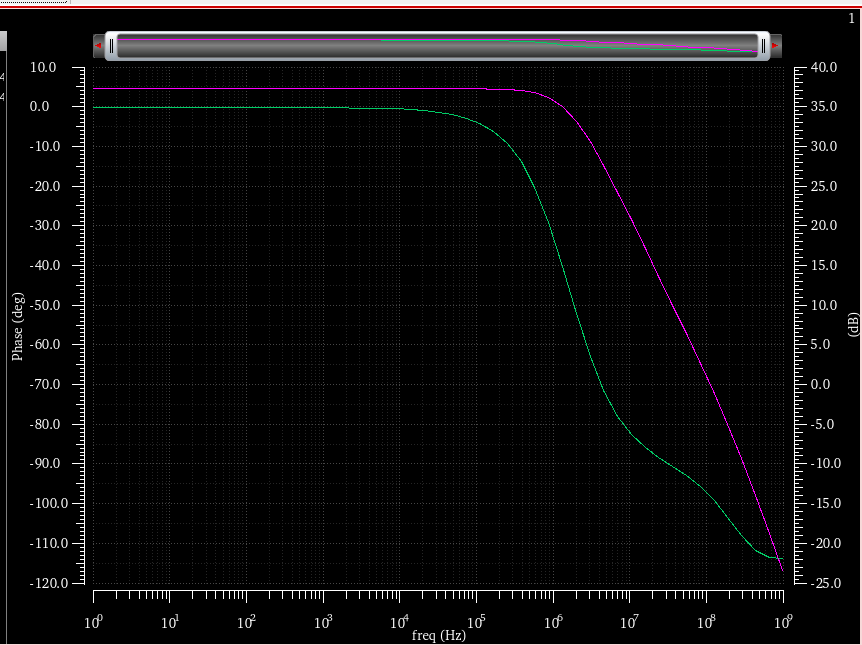
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Figure 13. Post simulation results 2

Comparing the former simulation results with the latter simulation results, the difference is not big, which indicates that the parasitic parameters have little influence, and the latter simulation passes.

Before, during and after the simulation is passed, and the design of the simulation part of this project is completed.

4、 Summary

This project completed the whole process design and Simulation of Analog IC differential amplifier. There are many problems encountered in the process of solving problems, also learned a lot of knowledge, increased experience. First of all, we should have solid theoretical knowledge as the foundation. For example, in the drawing of schematic diagram, the setting of transistor parameters is not tried out through repeated simulation failures. First of all, we should understand and use theoretical knowledge. First, we should set the transistor parameters in a reasonable area, and then test them through simulation, and fine tune them to achieve optimal performance. Secondly, according to the requirements of hierarchical circuit design, it is necessary to create a symbol for schematic diagram, which is not only convenient to define the port, but also convenient for other designers to call the designed module.

Finally, in the layout design and drawing, we should pay attention to the requirements of the process library. Although the layout design strives to reduce the area, we should also control the line width and spacing within the feasible range, and make as many through holes as possible. If the layout is changed, DRC and LVS should be verified again.

The simulation part of this project completed the whole process design of analog circuit through cadence platform. I am familiar with the design process and basic design methods of analog integrated circuits, and the use of cadence. I have made time and deduction for the theoretical knowledge learned in class, which has deepened my understanding of theoretical knowledge and the relationship between theoretical knowledge and practical design. The most important thing is to cultivate self-study ability. The most important thing is not knowledge itself, but continuous learning The process of knowledge.

Digital logic design

Induction lights are usually installed in the corridor to facilitate pedestrians while saving power. To design a corridor induction lamp control chip. There are four induction lights from downstairs to upstairs: lamp 1, lamp 2, lamp 3 and lamp 4. When pedestrians go up and down stairs, each lamp will automatically light up after sensing. If the induction signal disappears within 6S, it will be on for 6S. If the induction signal exists for more than 6S, the inductive signal will disappear and the lamp will turn off automatically after 3S. In order to avoid external interference misjudgment, if the induction signal duration is less than 0.3s, the induction lamp will not be turned on. In order to save energy, the last lamp will be turned off automatically within 0.5s after the next lamp is on (only one person's situation is considered).

The requirements are as follows:

Based on Modelsim or other EDA software, Verilog HDL language is used to complete the program editing and simulation verification. Key statements, modules or parameter variables should be clearly annotated.

**Steps and results**

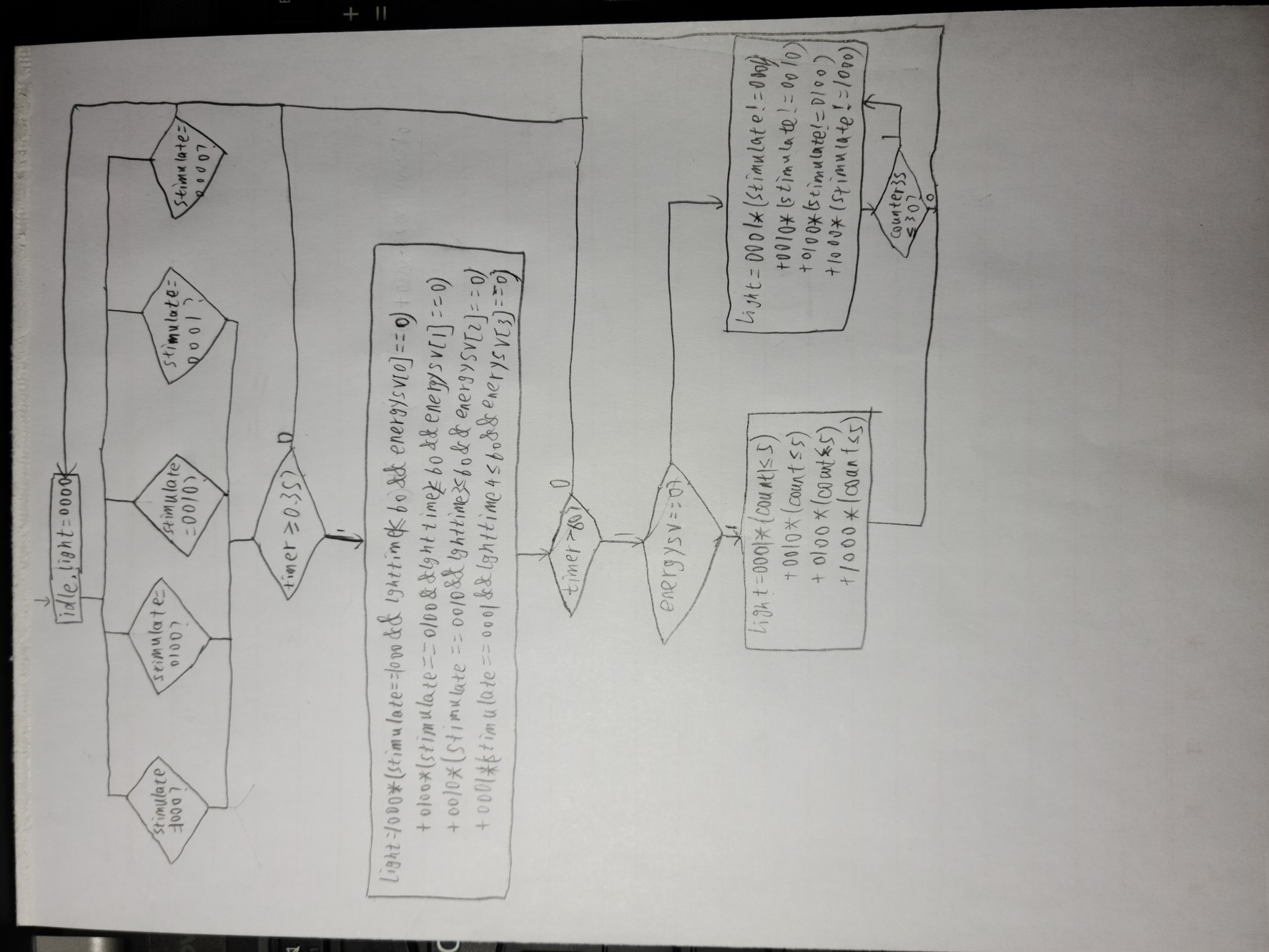
According to the requirements, draw a state transition diagram, as shown in Figure 14

Figure 14. State transition diagram

When the stimulus signal appears, first judge which floor it comes from. In order to prevent the interference signal, after the stimulus signal lasts for 0.3 seconds, the corresponding floor light will be turned on. After six seconds, whether the stimulus signal exists is more than six seconds, if it is more than six seconds, the light will continue to be on, and the light will be turned off 3 seconds after the stimulus signal disappears. At the same time, the lighting condition of other floors is monitored throughout the whole process. If the light is on, the energy-saving mode will be turned on, and the light of this floor will be turned off after 0.5 seconds.

The code and program description are attached in the appendix.

The simulation results are as follows

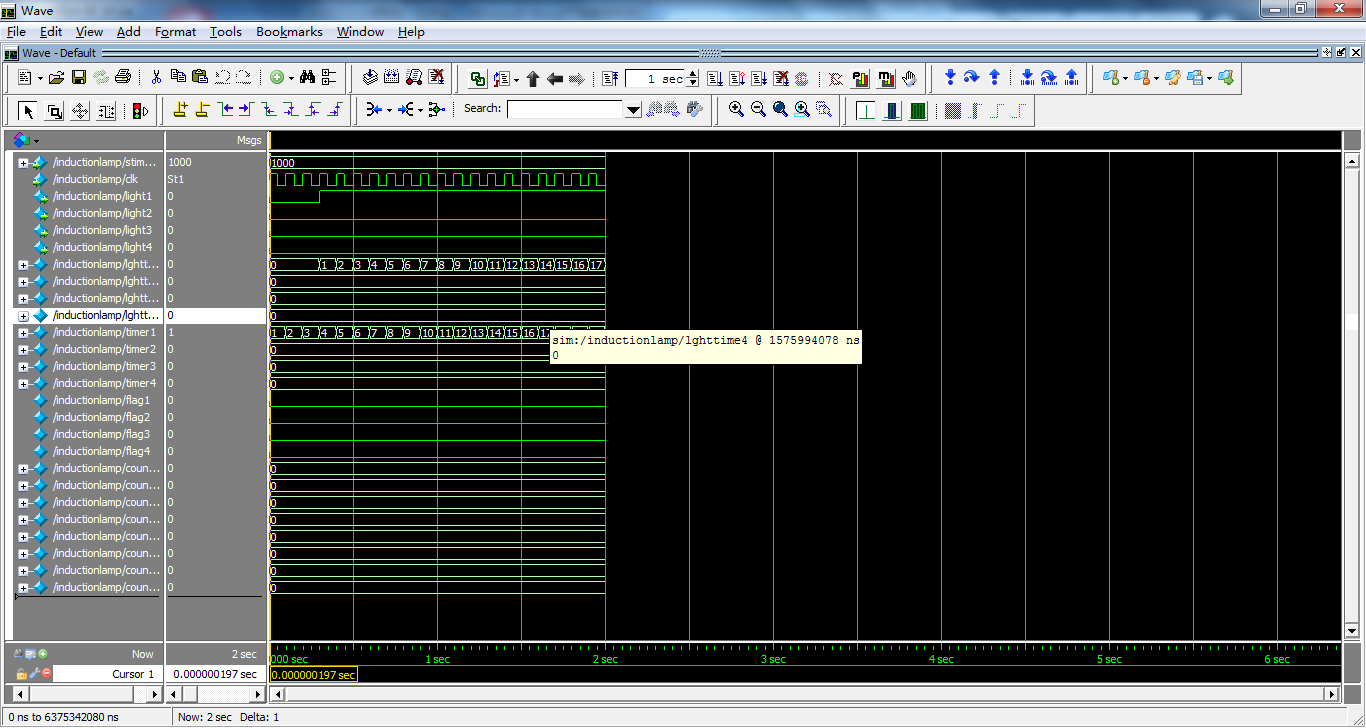
The simulation waveform is shown in the figure below: (in order to read the lighting time conveniently, the timer is reserved for checking, in which lghttime is the lighting time, and the timer starts timing from the appearance of stimulus signal, and the clock cycle is 0.1s.)

FIG. 15. The induction lamp lights up after the stimulation signal lasts for 0.3 seconds

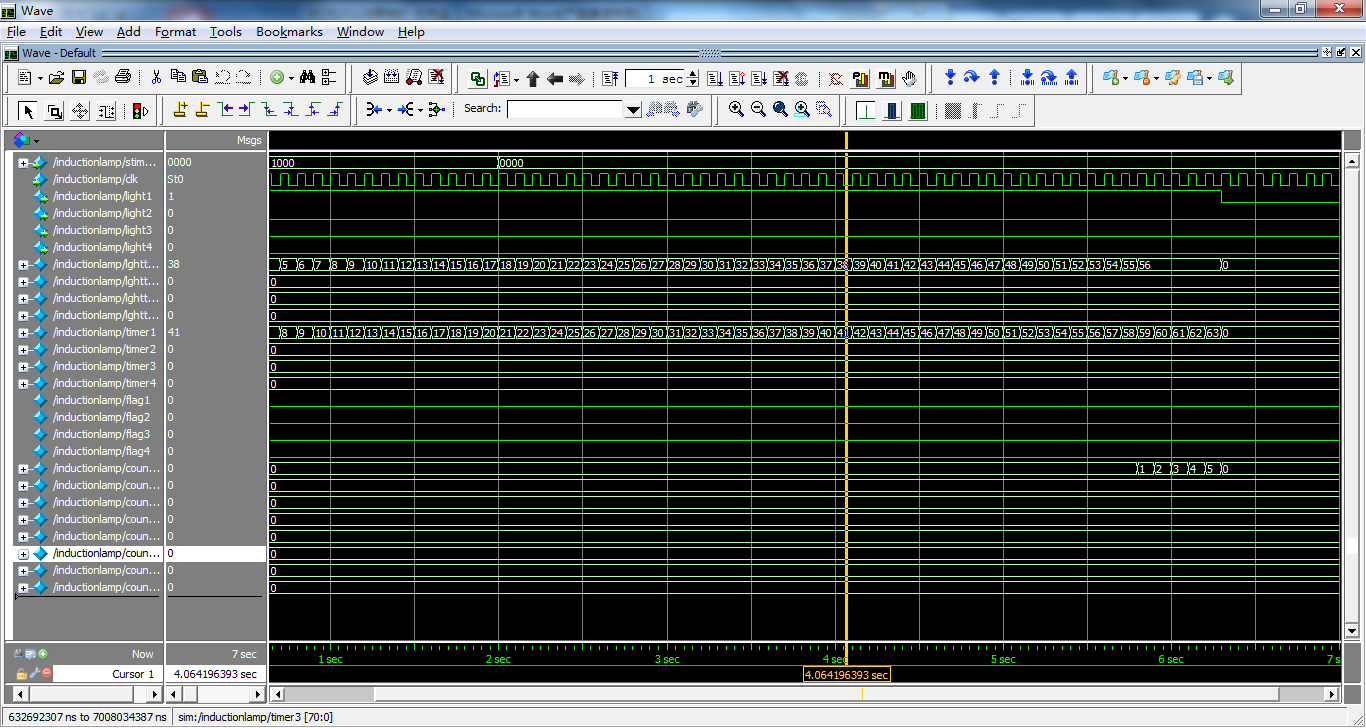


Figure 16. Stimulus signal did not last more than 6 seconds

Notice that Timer1 turns off the lights from 3 to 63. The lighting time is 6 seconds.

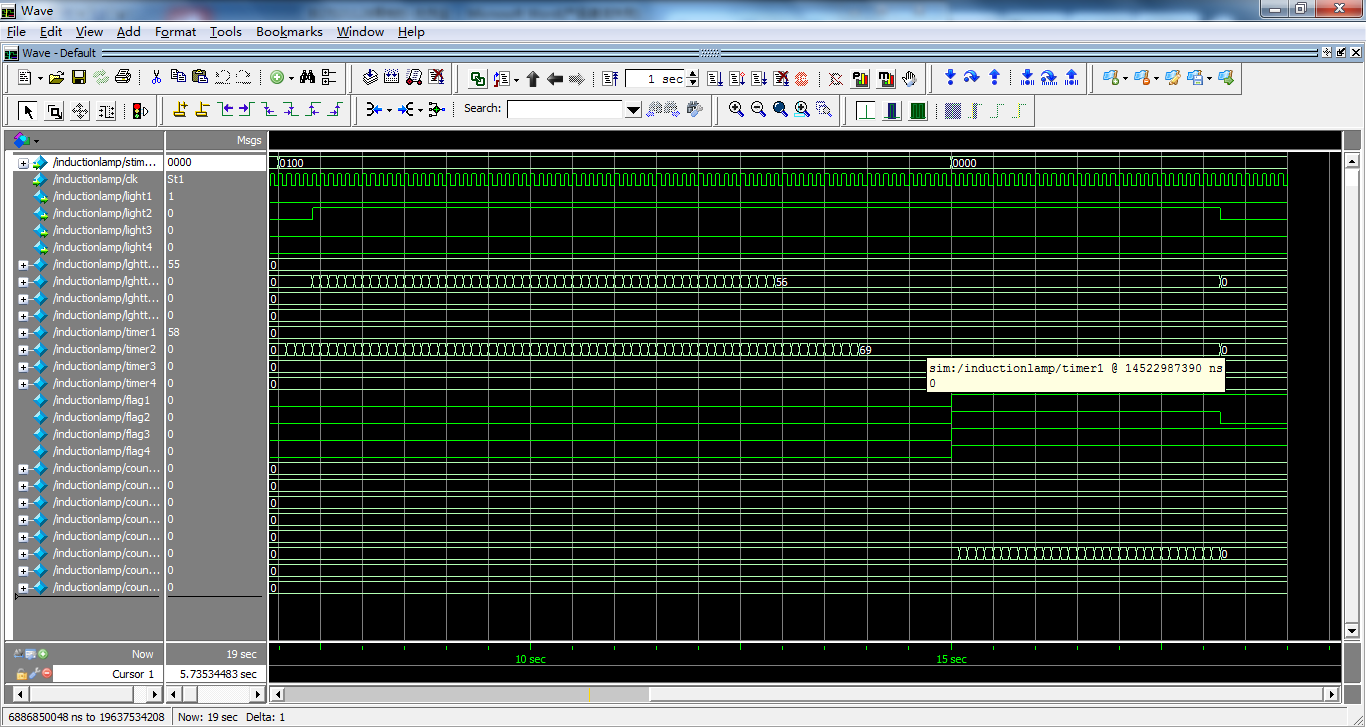


Figure 17. Inductive signal exists for more than 6 seconds

Wait for the sensing signal to disappear and turn off the light 3 seconds after the signal disappears.

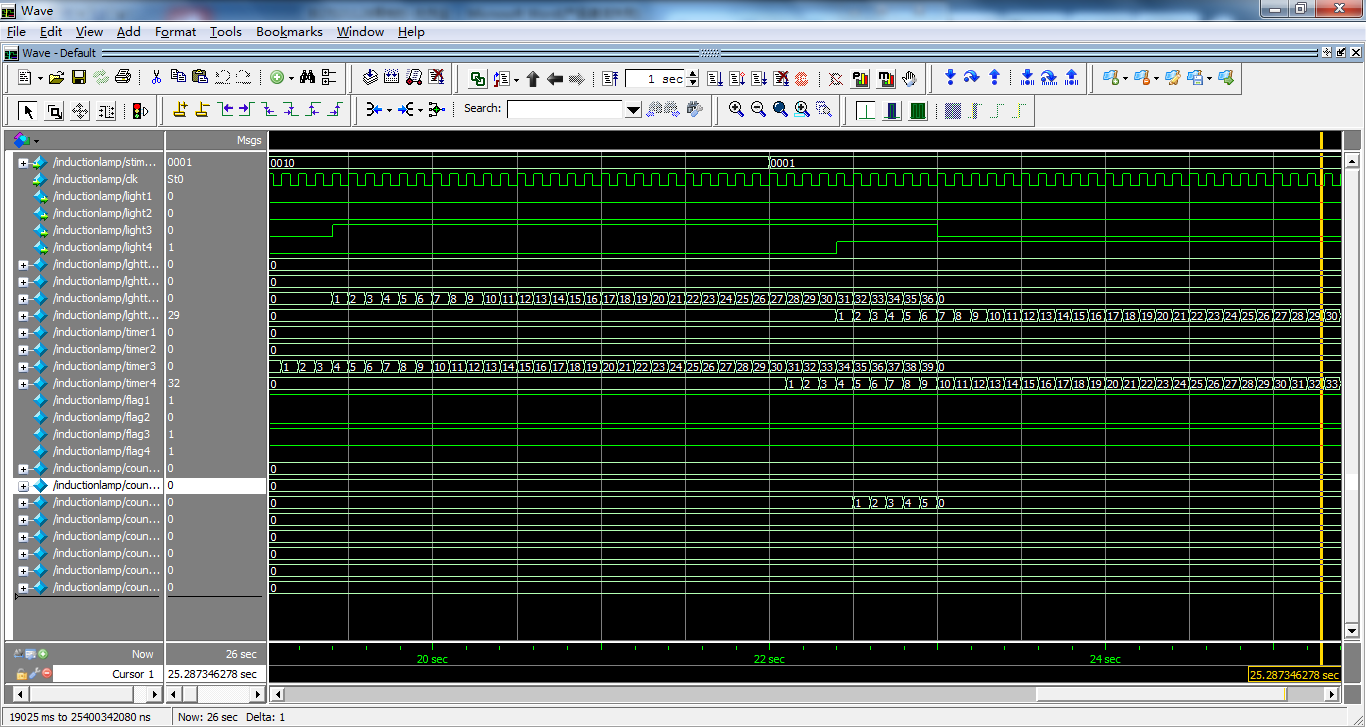


Fig. 18 simulation of energy saving mode within 6 seconds

First, the light on the third floor is turned on, and then a stimulus signal is added to the fourth floor. At this time, the program detects that the light on the fourth floor appears a rising edge during the lighting on the third floor, so it turns off the light on the third floor after 0.5 seconds.

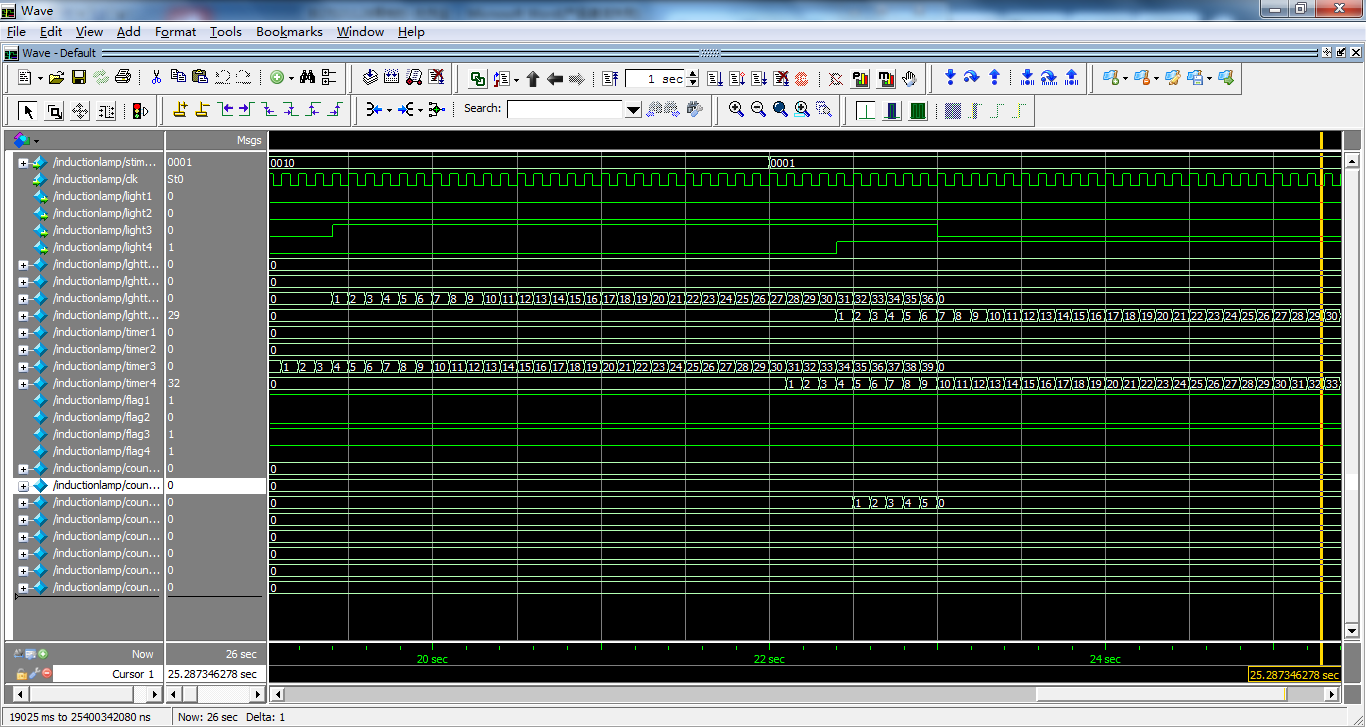


Fig. 19. Energy saving mode with stimulus signal for more than six seconds

When the stimulus signal exists for more than six seconds, the corresponding floor is still on, but the energy-saving mode is still considered. As can be seen from the figure, the stimulation signal still exists after six seconds, but at this time, the light on the third floor is turned on, so the energy-saving mode is entered, and the light on the fourth floor is turned off after 0.5 seconds.

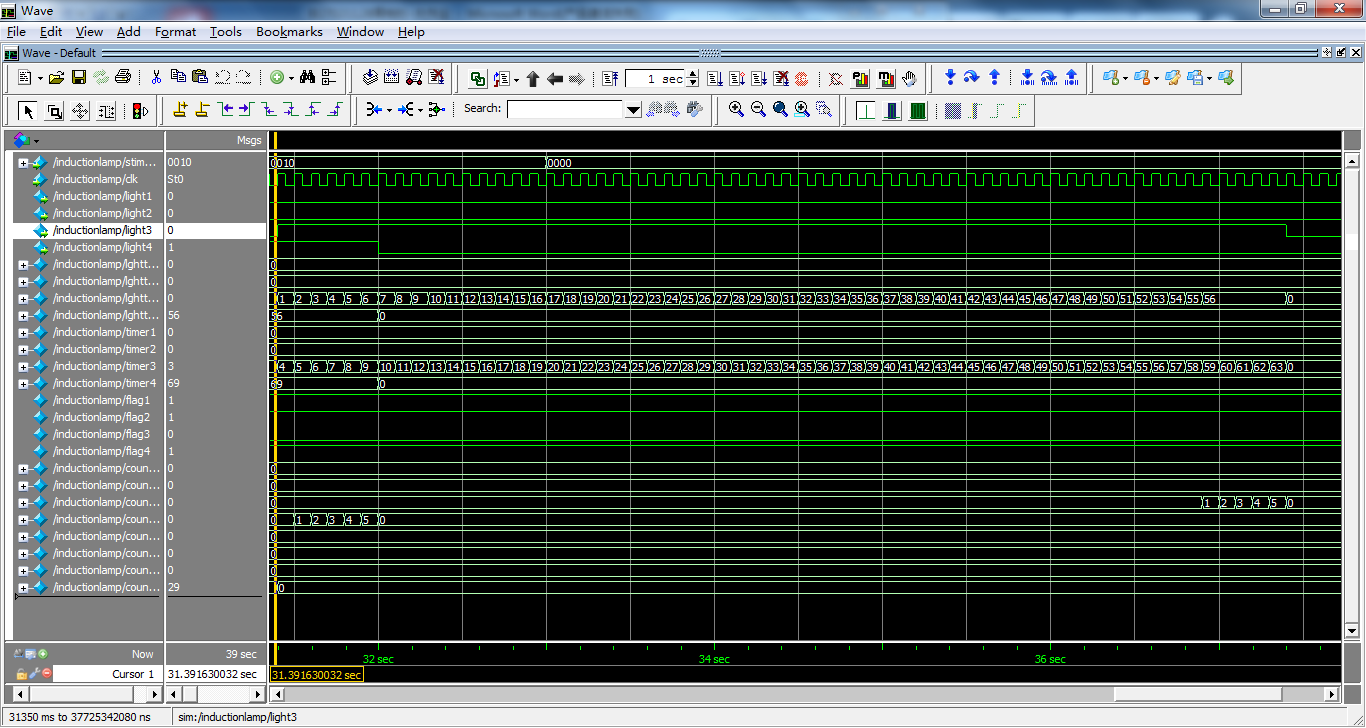


Figure 20. When the stimulus signal disappears, the light goes out after six seconds

**Code Description:**

First of all, the input clock of the module must be 0.1 second instead of 1 second. This has the advantages of speeding up the response speed of the induction lamp, and facilitating the timer to count decimal places. If the input clock period is not 100ms, an external frequency divider is needed, otherwise the unit of lighting time in corridor will not be in seconds.

When the stimulus duration is more than 0.3 seconds but less than 6 seconds, the light is on for three seconds. In the aspect of program implementation, two timers are used, timer is used to count the time when the stimulus signal appears, lghttime is used to time the light on, and two registers counter and counter 3S are used for timing. The function of counter is to generate a control signal to turn off the light of this layer after 0.5 seconds countdown when the energy-saving mode is on; the function of counter 3S is to save the stimulus signal When it is more than 6 seconds and disappears, the countdown starts for three seconds and a control signal is generated to turn off the lights on the floor. After the light is turned off, all relevant registers will be cleared and all control signals will be reset to prevent the next use.

Among them, the realization of energy-saving mode cannot be triggered by level information, but must be realized by using rising edge trigger. This is because only when the light of this floor is on, the lighting condition of adjacent floors can be monitored. When the lights of adjacent floors are on, it means that pedestrians have walked from this floor to adjacent floors, and then the lights of this floor can be turned off. If level sensitivity is used to control the switch signal of energy-saving mode, it will be impossible to distinguish which floor the pedestrian goes to first and then to which floor, thus it is impossible to determine which floor will enter the energy-saving mode.

**Summary for digital part**

In this project, the design and Simulation of the digital front-end are completed. It involves a lot of related knowledge, such as digital system design process, Verilog syntax, structure and so on. Some Verilog syntax is used, such as if else structure, Boolean expression and always block, which deepens my understanding of Verilog syntax. Among them, the begin end block is a sequential block, in which the statement order is executed from top to bottom, and the fork join block is a parallel block. The statements in the block are executed at the same time, or delay statements such as "10" can be added to the execution order of the statements in the parallel block Sort. Secondly, the initial module is executed only once. A module can have multiple always blocks, but the always blocks cannot be nested. The always blocks run in parallel at the same time. Each always block monitors the key signals. The energy-saving function in the program needs to realize an asynchronous reset function, which is realized by multiple always blocks. It needs multiple always blocks to monitor the sensitive signal, and then change the value of the control signal to control the registers in other always blocks. At the same time, the values of registers in always block can only be assigned by non-blocking, that is, the value of registers will be changed after the end of the clock cycle, which is similar to the post + + operation in C + + language.

I am familiar with many kinds of digital grammar, and use the digital language to enhance my ability to design the system.